

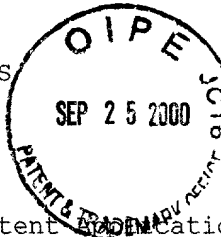
THE COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

Docket No. TS2000-143

Sir:



09/25/00



jc525 U.S. PTO
09/669159
09/25/00

Transmitted herewith for filing is the Patent Application of:

Inventor: **HORNG-WEN CHEN AND CHI-HOW WU**

For: **AN IN-SITU STRIP PROCESS FOR POLYSILICON ETCHING IN DEEP SUB-MICRON TECHNOLOGY**

Enclosed are:

- ☒ 6 sheets of drawing(s) - formal.
- ☒ An assignment of the invention to **Taiwan Semiconductor Manufacturing Company**
- ☐ An associate power of attorney

The filing fee has been calculated as shown below:

	(Col. 1)	(Col. 2)	OTHER THAN A SMALL ENTITY	
FOR:	NO. FILED	NO. EXTRA	RATE	FEE
BASIC FEE				\$ 690.
TOTAL CLAIMS	20 -20=	0	x 18 =	\$ 0.
INDEP CLAIMS	3 -3=	0	x 78 =	\$ 0.
MULTIPLE DEPENDENT CLAIM PRESENTED			+ 260 =	
			SUB TOTAL	\$ 690.
			ASSIGNMENT	\$40.
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- ☒ Please charge my Deposit Account No. 19-0033 in the amount of \$ 730. A duplicate copy of this sheet is enclosed.
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Respectfully submitted,


STEPHEN B. ACKERMAN, REG. NO. 37,761



AN IN-SITU STRIP PROCESS FOR POLYSILICON ETCHING
IN DEEP SUB-MICRON TECHNOLOGY

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to a method of fabricating semiconductor structures, and more particularly, to a method of patterning a polysilicon layer in the manufacture of an integrated circuit device.

(2) Description of the Prior Art

Polysilicon pattern definition remains a significant challenge in semiconductor manufacturing. The minimum width of the polysilicon layer determines the minimum transistor length of MOS technologies. Transistor switching speed and packing density depend heavily on the ability to reliably and repeatably manufacture transistors with very narrow polysilicon gates.

Referring now to Fig. 1, a cross-section of a partially completed prior art integrated circuit device is

shown. A gate oxide layer 14 overlies a semiconductor substrate 10. A polysilicon layer 18 overlies the gate oxide layer 14. A hard mask layer 22 overlies the polysilicon layer 18. Finally, a photoresist layer 26 overlies the hard mask layer 22. Note that the photoresist layer 26 has been patterned by, for example, a photolithographic sequence of coating, exposure, and development.

Referring now to Fig. 7, the polysilicon layer 18 is patterned using the prior art sequence that is illustrated by the process flow chart. Note, first, that the prior art process etches the pattern of the photoresist layer 26 into the hard mask layer 22 in step 30. Second, the photoresist layer 26 is stripped away in step 34. Third, the pattern of the hard mask layer 22 is etched into the polysilicon layer 18 in step 38. Finally, the hard mask layer 22 is stripped away in step 42. Note that an intervening resist strip (step 34) necessitates the removal of the wafers from the etching chamber between the hard mask etch (step 30) and the gate etch (step 38).

Referring now to Fig. 2 and to Fig. 7, step 30, the photoresist layer 26 may be trimmed. This trimming step is

performed to reduce the width of the photoresist layer 26 to a dimension that is smaller than the capability of the photolithographic exposure equipment. This trimming etch is performed in the plasma dry etch chamber and reduces the width of the patterned photoresist layer 26 to a dimension that will enable the final patterned polysilicon layer 18 to meet the critical dimension (CD) specifications for the manufacturing process.

Referring now to Fig. 3 and to Fig. 7, step 30, the pattern of the photoresist layer 26 is etched into the hard mask layer 22. This etching step is again performed in the plasma dry etch chamber.

Referring now to Fig. 4 and to Fig. 7, step 34, the photoresist layer 26 is stripped away. This photoresist layer 26 must be removed to improve the selectivity of the plasma dry etch process. Because the gate oxide layer 14 of the deep sub-micron process is very thin, the subsequent polysilicon etching step must have a high selectivity to the gate oxide. Removing the photoresist layer 26 prior to the polysilicon etch step 38 improves this selectivity. This is the reason that the hard mask layer 22 is used.

Of particular importance to the present invention is the fact that the semiconductor wafers must be removed from the plasma dry etch chamber during photoresist stripping. A separate photoresist stripping chamber is typically used to strip away this remaining photoresist. Following the photoresist strip, the wafers are then returned to the plasma dry etch chamber for the gate or polysilicon layer 18 etch step 38. This polysilicon layer 18 is thereby etched in a photoresist free process that is herein called an ex-situ process.

The additional wafer handling and process equipment required to remove the photoresist layer 26 increases the cycle time and the processing cost. In addition, the wafers are open to increased contamination due to the handling and the additional processing chamber. The additional processing chamber also makes controlling processing parameters more difficult. Finally, additional inspections and CD measurement steps may be added to insure that the additional handling and process set-ups are within specification. This also adds to the processing cost and cycle time.

Referring now to Fig. 5 and to Fig. 7, step 38, the pattern of the hard mask layer 22 is etched into the polysilicon layer 18. This step is performed in the plasma dry etch chamber after the photoresist strip step 34.

Referring finally to Fig. 6 and to Fig. 7, step 42, the hard mask layer is stripped away to complete the patterning of the polysilicon layer 18. The wafers are removed from the plasma dry etch chamber for this processing step 42. The hard mask stripping may comprise a wet etch process.

Several prior art approaches disclose methods to pattern polysilicon in the manufacture of an integrated circuit device. U.S. 5,767,018 to Bell teaches a method to etch a polysilicon pattern where an anti-reflective coating (ARC) is used. Pitting problems are eliminated. In one embodiment, a passivation layer is formed on the sidewalls of the patterned ARC layer prior to polysilicon etching. In a second embodiment, the passivation layer is formed on the ARC layer sidewalls during the polysilicon etch. U.S. Patent 6,037,266 to Tao et al discloses a method to etch a polysilicon pattern. A bottom anti-reflective coating (BARC) is used. The BARC layer and an oxide layer are

etched to form a pattern over the polysilicon layer. The BARC layer is then stripped away using a biased O₂ plasma. The polysilicon layer is then etched using the oxide layer as a hard mask. U.S. Patent 5,346,586 to Keller teaches a method to etch a polysilicon pattern. A silicide layer is used overlying the polysilicon layer. An oxide layer overlies the silicide layer. The oxide layer is patterned using a photoresist layer. The photoresist layer is then removed using an ozone plasma strip. The silicide layer is etched. Finally, the polysilicon layer is etched. U.S. Patent 5,885,902 to Blasingame et al discloses a method to etch an anti-reflective coating (ARC) layer using an inert gaseous plasma containing helium, nitrogen, or a mixture thereof.

SUMMARY OF THE INVENTION

A principal object of the present invention is to provide an effective and very manufacturable method of patterning a polysilicon layer in the manufacture of an integrated circuit device.

A further object of the present invention is to provide a method to pattern the polysilicon layer that reduces process cycle time in the processing sequence.

Another further object of the present invention is to provide a method to pattern the polysilicon layer that reduces wafer handling.

A yet further object of the present invention is to provide a method to pattern the polysilicon layer by stripping away the photoresist layer in-situ to the polysilicon dry plasma etch chamber.

A still further object of the present invention is to provide a method to eliminate photoresist polymer residue from the polysilicon dry etch chamber.

In accordance with the objects of this invention, a new method of patterning the polysilicon layer in the manufacture of an integrated circuit device has been achieved. A polysilicon layer is provided overlying a semiconductor substrate. The polysilicon layer may overlie a gate oxide layer and would thereby comprise the polysilicon gate for MOS devices. A hard mask layer is

provided overlying the polysilicon layer. A resist layer is provided overlying the hard mask layer. The resist layer is patterned to form a resist mask the exposes a part of the hard mask layer. The polysilicon layer is patterned in a plasma dry etching chamber. First, the resist layer is optionally trimmed by etching. Second, the hard mask layer is etched where exposed by the resist mask to form a hard mask that exposes a part of the polysilicon layer. Third, the resist mask is stripped away. Fourth, polymer residue from the resist mask is cleaned away using a chemistry containing CF_4 gas. Fifth, the polysilicon layer is etched where exposed by the hard mask. After the polysilicon layer is so patterned in the dry plasma etch chamber, the hard mask layer is stripped away to complete the patterning of the polysilicon layer in the manufacture of the integrated circuit device.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

Figs. 1 through 6 illustrate in cross-section a partially completed prior art integrated circuit device.

Fig. 7 illustrates the process flow sequence for the prior art polysilicon patterning method.

Fig. 8 illustrates the process flow sequence for the preferred embodiment of the method of the present invention.

Figs. 9 through 12 illustrate in cross-section the preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The embodiment discloses the application of the present invention to the patterning of the polysilicon layer in the manufacture of an integrated circuit device. It should be clear to those experienced in the art that the present invention can be applied and extended without deviating from the scope of the present invention.

Referring now particularly to Fig. 8, a process flow sequence for the preferred embodiment of the present invention is shown. This process flow is of particular importance to the present invention. In the preferred process flow, the resist trim etch, hard mask etch, resist strip, and gate etch are combined into a single process step 50 within a dry plasma etch chamber. The novel method allows these processing components to be conducted using a continuous dry plasma etching recipe through the sequential introduction of gases and control of parameters. The cost, time consumption, and contamination that are introduced by the excessive wafer handling of the prior art process are thereby eliminated. After the polysilicon layer, herein called the gate, is etched, the wafers may be removed from the dry plasma etch chamber. The hard mask layer is then stripped in step 54.

As in the prior art process, the resist trim step is optional to the method of the invention. The resist trim step may be used to reduce the line width of the photoresist layer beyond the capability limits of the photolithographic equipment.

Of particular importance to the process flow is the inclusion within the etching step 50 of a polymer clean step. After the resist layer is stripped away, residual organic polymer from the resist material may be present in the chamber and on the sidewalls of the hard mask. A polymer cleaning is therefore an essential aspect of the present invention. The organic polymer is removed using a cleaning chemistry containing CF_4 gas. The chamber and the integrated circuit device is thereby cleaned of residual organic polymer material prior to the critical polysilicon gate etch.

Referring now to Fig. 9, a cross-section of the partially completed device of the present invention method is shown. A semiconductor substrate 60 is provided. The semiconductor substrate preferably comprises monocrystalline silicon. A gate oxide layer 64 is provided overlying the semiconductor substrate 60. The gate oxide layer 64 is very thin in a deep sub-micron MOS process. For example, the gate oxide layer 64 is formed by conventional means to about 20 Angstroms.

A polysilicon layer 68 is provided overlying the gate oxide layer 64. The polysilicon layer 68 may be doped or

undoped and is formed by conventional means. As an example, the polysilicon of the preferred embodiment is undoped and has a thickness of between about 1,500 Angstroms and 2,500 Angstroms.

A hard mask layer 72 is provided overlying the polysilicon layer 68. The hard mask layer 72 will subsequently be patterned to form a hard mask overlying the polysilicon layer 68 for the polysilicon etch step. The hard mask layer 72 preferably comprises silicon oxynitride with a thickness of between about 300 Angstroms and 500 Angstroms. Silicon dioxide could be used as the hard mask layer 72 in the present invention.

A silicon dioxide layer 76 is provided overlying the hard mask layer 72. The silicon dioxide layer 76 is used as a buffer layer to gain etching selectivity during the polysilicon etching. The silicon dioxide layer 76 is optional to the present invention.

A resist layer 80 is provided overlying the silicon dioxide layer 76. The resist layer 80 preferably comprises a conventional photoresist material that has been applied, exposed and developed to form a pattern. The resist layer

80 thereby contains the pattern that will be transferred, first, to the hard mask layer 72 and, second, to the polysilicon layer 68. As an example, the preferred resist layer 80 comprises a deep ultra-violet (DUV) photoresist, such as ShinEtsu 233DT. The photoresist material is spin coated overlying the wafer to a thickness of between about 3,500 Angstroms and 5,000 Angstroms. Following bake, the resist layer has a thickness of between about 3,000 Angstroms and 4,700 Angstroms. The resist layer 80 is patterned, for example, to a minimum line with critical dimension (CD) of between about 0.151 microns and 0.169 microns.

Referring now to Fig. 10, several important features of the present invention are presented. The semiconductor wafers are loaded into the dry etching chamber as outlined in the process flow step 50. In the preferred process example, the dry plasma etching chamber comprises an Applied Materials DPS-POLY system. The overall dry plasma etching recipe sequence, shown as step 50 of Fig. 8, comprises a series of recipe steps. Each recipe step completes a step in the process of transferring the resist layer pattern into the polysilicon layer.

The first recipe step comprises the trim etch. As in the prior art process, the trimming step is not considered an essential aspect of the method of the present invention. In the trimming etch, the resist layer 80 is etched to reduce the line widths of the resist layer 80. In the example process, the minimum pre-trim resist layer 80 width is between about 0.151 microns and 0.169 microns. The final after etch polysilicon CD is specified at between about 0.145 microns and 0.125 microns. Since the final polysilicon CD is about 0.025 microns less than the available resist CD, it is necessary to trim back the width of the resist layer 80.

The trimming etch recipe preferably comprises a combination of gases. In the preferred embodiment, HBr gas is flowing at a rate of between about 60 sccm and 100 sccm, Ar gas is flowing at a rate of between about 40 sccm and 80 sccm, and O₂ gas is flowing at a rate of between about 2 sccm and 10 sccm. The chamber pressure is between about 4 milliTorr and 15 milliTorr. A source power of between about 200 Watts and 400 Watts and a bias power of between about 40 Watts and 80 Watts are used. The trimming etch is performed for between about 20 seconds and 60 seconds. The trimming etch reduces the width of the resist layer 80

prior to transferring the pattern to the hard mask layer 72.

Following the trim etch, the hard mask layer 72 is etched. If the silicon dioxide layer 76 is used, it is etched with the hard mask layer. The hard mask etch comprises a combination of gases. In the preferred embodiment, CF_4 gas is flowing at a rate of between about 10 sccm and 30 sccm and Ar gas is flowing at a rate of between about 140 sccm and 160 sccm. The chamber pressure is maintained at between about 8 milliTorr and 12 milliTorr. The source power is controlled at between about 550 Watts and 650 Watts while the bias power is controlled at between about 40 Watts and 80 Watts. The hard mask layer 72 is etched using an endpoint detection that detects when the hard mask layer 72 has been etched through.

Following the hard mask etch, the resist layer 80 is stripped away. The ability to perform this step within the same dry etch plasma chamber is an important feature of the present invention. The resist layer 80 is removed by flowing O_2 gas at a rate of between about 40 sccm and 60 sccm. A chamber pressure of between about 4 milliTorr and 15 milliTorr is maintained. The source power is controlled

at between about 300 Watts and 500 Watts, while the bias power is controlled at between about 80 Watts and 100 Watts. The strip is stopped using an endpoint detection that detects that the photoresist layer 80 is no longer present.

Following the resist strip step, it is likely that organic polymer residue remains from the photoresist material. This residue will coat the interior of the dry plasma etching chamber and may adhere to the sidewalls of the hard mask 72 and 76 as shown by 84 in Fig. 10. It is critical to the method of the present invention that the resist stripping step be followed by a polymer cleaning step. The polymer clean removes any organic polymer residue from the chamber and from the sidewalls of the hard mask 72 and 76.

The polymer clean step is accomplished by flowing CF_4 gas at a rate of between about 60 sccm and 100 sccm. The chamber pressure is maintained at between about 4 milliTorr and 15 milliTorr. The source power is controlled at between about 300 Watts and 500 Watts, while the bias power is controlled at between about 30 Watts and 50 Watts. The polymer clean is performed for between about 5 seconds and

15 seconds. The polymer cleaning step keeps the chamber clean prior to each polysilicon etch process.

Referring now to Fig. 11, the polysilicon layer 68 is now etched using two recipe steps comprising, first, a main etch (ME) and, second, an overetch (OE). In the main etch, the polysilicon layer 68 is etched using a gas combination of HBr, Cl₂, and He-O₂. The main etch is stopped using an endpoint detection method that detects when the polysilicon layer 68 has been etched through. The overetch recipe uses a gas combination of HBr and He-O₂ for a controlled time period to insure that the remaining polysilicon layer 68 will be free of stringers and shorts.

The main etch comprises HBr flowing at a rate of between about 160 sccm and 200 sccm, Cl₂ flowing at a rate of between about 10 sccm and 30 sccm, and He-O₂ flowing at a rate of between about 2 sccm and 10 sccm. The chamber pressure is maintained at between about 4 milliTorr and 15 milliTorr. The source power is controlled at between about 550 Watts and 650 Watts. The bias power is controlled at between about 30 Watts and 50 Watts.

The overetch recipe comprises HBr flowing at a rate of between about 130 sccm and 150 sccm and He-O₂ flowing at a rate of between about 4 sccm and 6 sccm. The chamber pressure is maintained at between about 60 milliTorr and 100 milliTorr. The source power is controlled at between about 300 Watts and 500 Watts, while the bias power is controlled at between about 60 Watts and 80 Watts. The overetch is performed for between about 60 seconds and 100 seconds. Following the polysilicon etch, the device cross-section appears as shown in Fig. 11. The silicon dioxide layer 76 is etched away during the polysilicon etch step.

Referring now to Fig. 12, the hard mask is stripped away to complete the patterning of the polysilicon layer 68. The wafers are removed from the dry plasma etch chamber to perform the hard mask strip. In the preferred embodiment, the hard mask layer 72 comprises silicon oxynitride. This silicon oxynitride layer 72 is preferably removed using a wet etch comprising H₃PO₄.

The method of the present invention, using the in-situ stripping of the photoresist layer, has been demonstrated on a 0.15 micron process. The method demonstrates stable

after etch inspection (AEI) CD performance. The three-sigma variation is between about 4 nanometers and 8 nanometers. SEM and X-SEM profiles, after polysilicon gate etching, demonstrate excellent vertical profiles with no pitting, trenching, or residue problems. In addition, the method saves about 4 hours compared to the prior art approach.

As shown in the preferred embodiments, the present invention provides a very manufacturable process for patterning the polysilicon layer in an integrated circuit device. The present invention saves cycle time and reduces costs. The present invention has been successfully demonstrated on a 0.15 micron process. The novel approach allows photoresist to be stripped away in the dry plasma etch chamber. The polymer cleaning step eliminates problems associated with resist residue build-up in the chamber or on hard mask sidewalls.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made

without departing from the spirit and scope of the invention.

What is claimed is:

1. A method to pattern a polysilicon layer in the manufacture of an integrated circuit device comprising:

providing a polysilicon layer overlying a semiconductor substrate;

5 providing a hard mask layer overlying said polysilicon layer;

providing a resist layer overlying said hard mask layer;

patterning said resist layer to form a resist mask that exposes a part of said hard mask layer;

10 patterning said polysilicon layer wherein said patterning is performed sequentially in a dry plasma etch chamber and wherein said patterning comprises:

etching said hard mask layer exposed by said resist mask to form a hard mask that exposes a part of said polysilicon layer;

15 thereafter stripping away said resist mask;

thereafter cleaning away polymer residue from said resist mask wherein said cleaning away comprises a chemistry containing CF_4 gas; and

20 thereafter etching said polysilicon layer exposed by said hard mask; and

stripping away said hard mask to complete the patterning of said polysilicon layer in the manufacture of the integrated circuit device.

2. The method according to Claim 1 wherein said hard mask layer comprises silicon oxynitride.

3. The method according to Claim 1 wherein said step of etching said hard mask layer comprises a chemistry containing CF_4 gas.

4. The method according to Claim 1 wherein said step of stripping away said resist mask comprises a chemistry containing O_2 gas.

5. The method according to Claim 1 wherein said step of etching said polysilicon layer comprises a main etch step followed by an overetch step.

6. The method according to Claim 1 wherein said step of etching said polysilicon layer comprises a chemistry of: HBr gas, Cl_2 gas, He-O_2 gas, and combinations thereof.

7. The method according to Claim 1 further comprising providing a silicon dioxide layer overlying said hard mask layer and underlying said resist layer.

8. The method according to Claim 1 further comprising etching

said resist layer to trim said resist layer prior to said step of etching said hard mask layer wherein said etching of said resist layer is performed in said dry plasma etching chamber.

9. A method to pattern a polysilicon layer in the manufacture of an integrated circuit device comprising:

providing a polysilicon layer overlying a semiconductor substrate;

5 providing a hard mask layer overlying said polysilicon layer;

providing a resist layer overlying said hard mask layer;

patterning said resist layer to form a resist mask that exposes a part of said hard mask layer;

10 patterning said polysilicon layer wherein said patterning is performed sequentially in a dry plasma etch chamber and wherein said patterning comprises:

etching said resist mask to trim said resist mask;

15 thereafter etching said hard mask layer exposed by said resist mask to form a hard mask that exposes a part of said polysilicon layer;

thereafter stripping away said resist mask;

20 thereafter cleaning away polymer residue from said resist mask wherein said cleaning away comprises a chemistry containing CF_4 gas; and

thereafter etching said polysilicon layer exposed by
said hard mask; and

stripping away said hard mask to complete the patterning
of said polysilicon layer in the manufacture of the integrated
25 circuit device.

10. The method according to Claim 9 wherein said hard mask
layer comprises silicon oxynitride.

11. The method according to Claim 9 wherein said step of
etching said resist mask to trim said resist mask comprises a
chemistry containing O₂ gas.

12. The method according to Claim 9 wherein said step of
etching said hard mask layer comprises a chemistry of CF₄ gas.

13. The method according to Claim 9 wherein said step of
stripping away said resist layer comprises a chemistry
containing O₂ gas.

14. The method according to Claim 9 wherein said step of
etching said polysilicon layer comprises a main etch step
followed by an overetch step.

15. The method according to Claim 9 wherein said step of

etching said polysilicon layer comprises a chemistry of: HBr gas, Cl₂ gas, He-O₂ gas, and combinations thereof.

16. The method according to Claim 1 further comprising providing a silicon dioxide layer overlying said hard mask layer and underlying said resist layer.

17. A method to pattern a polysilicon layer in the manufacture of an integrated circuit device comprising:

providing a gate oxide layer overlying a semiconductor substrate;

5 providing a polysilicon layer overlying said gate oxide layer;

providing a silicon oxynitride layer overlying said polysilicon layer;

10 providing a silicon dioxide layer overlying said silicon dioxide layer;

providing a resist layer overlying said silicon dioxide layer;

patterning said resist layer to form a resist mask that exposes a part of said silicon oxynitride layer;

15 patterning said polysilicon layer wherein said patterning is performed sequentially in a dry plasma etch chamber and wherein said patterning comprises:

etching said resist mask to trim said resist mask;

thereafter etching said silicon dioxide layer and
20 said silicon oxynitride layer exposed by said resist mask
to form a hard mask that exposes a part of said
polysilicon layer;

thereafter stripping away said resist mask;

thereafter cleaning away polymer residue from said
25 resist mask wherein said cleaning away comprises a
chemistry containing CF_4 gas; and

thereafter etching said polysilicon layer exposed by
said hard mask wherein said etching comprises a main etch
step followed by an overetch step; and

30 stripping away said hard mask to complete the patterning
of said polysilicon layer in the manufacture of the integrated
circuit device.

18. The method according to Claim 17 wherein said step of
etching said silicon dioxide layer and said silicon oxynitride
layer comprises a chemistry of CF_4 gas.

19. The method according to Claim 17 wherein said step of
stripping away said resist layer comprises a chemistry
containing O_2 gas.

20. The method according to Claim 17 wherein said step of

etching said polysilicon layer comprises a chemistry of: HBr gas, Cl_2 gas, He- O_2 gas, and combinations thereof.

ABSTRACT

A new method of patterning the polysilicon layer in the manufacture of an integrated circuit device has been achieved. A polysilicon layer is provided overlying a semiconductor substrate. The polysilicon layer may overlie a gate oxide layer and thereby comprise the polysilicon gate for MOS devices. A hard mask layer is provided overlying the polysilicon layer. A resist layer is provided overlying the hard mask layer. The resist layer is patterned to form a resist mask that exposes a part of the hard mask layer. The polysilicon layer is patterned in a plasma dry etching chamber. First, the resist layer is optionally trimmed by etching. Second, the hard mask layer is etched where exposed by the resist mask to form a hard mask that exposes a part of the polysilicon layer. Third, the resist mask is stripped away. Fourth, polymer residue from the resist mask is cleaned away using a chemistry containing CF_4 gas. Fifth, the polysilicon layer is etched where exposed by the hard mask. After the polysilicon layer is so patterned in the dry plasma etch chamber, the hard mask layer is stripped away to complete the patterning of the polysilicon layer in the manufacture of the integrated circuit device.

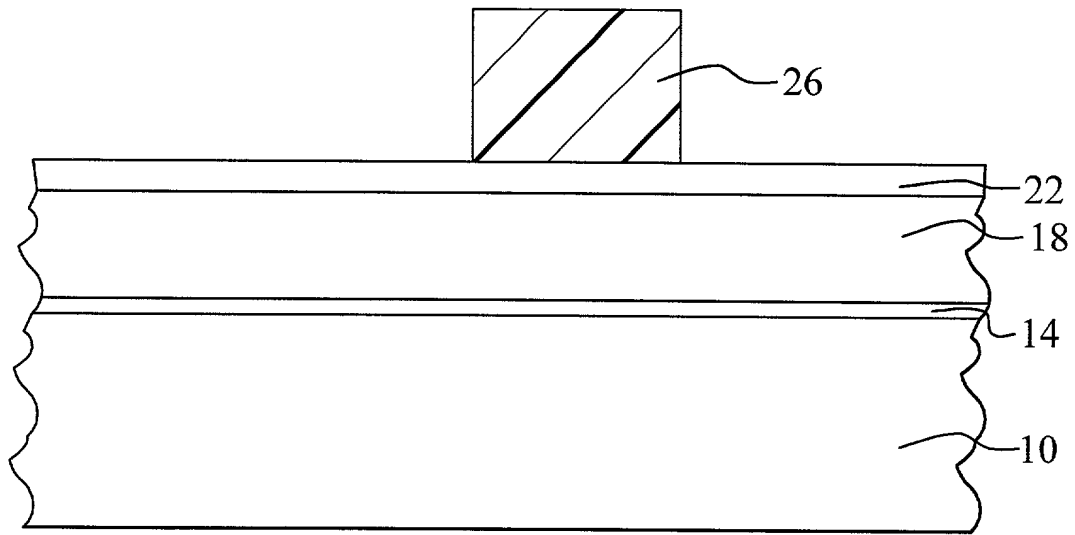


FIG. 1 Prior Art

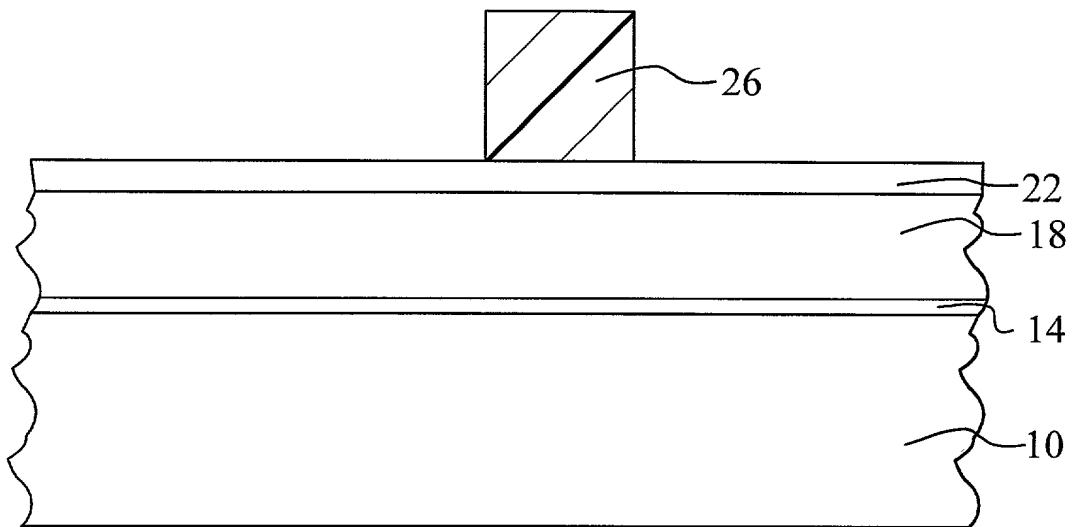


FIG. 2 Prior Art

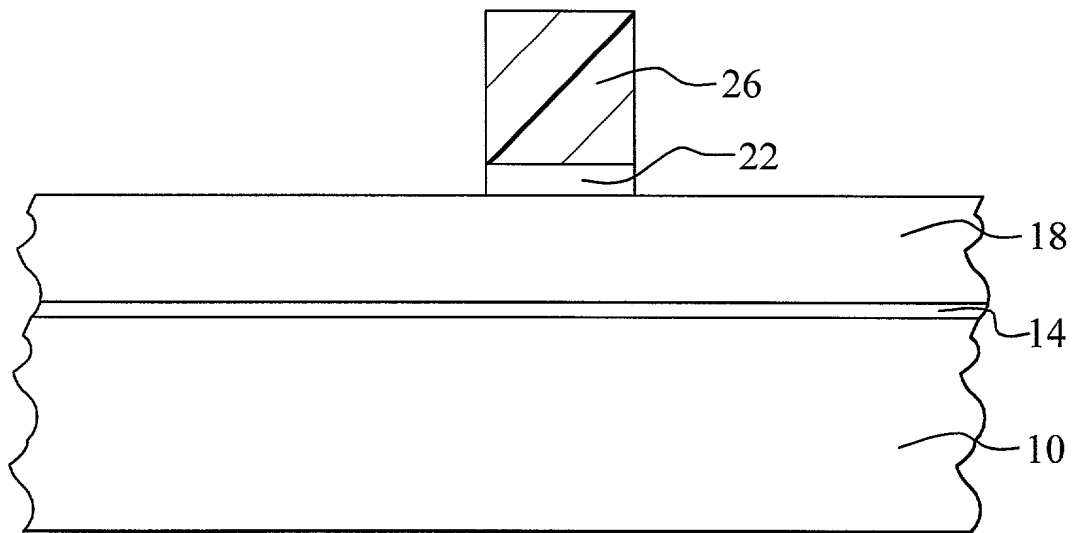


FIG. 3 Prior Art

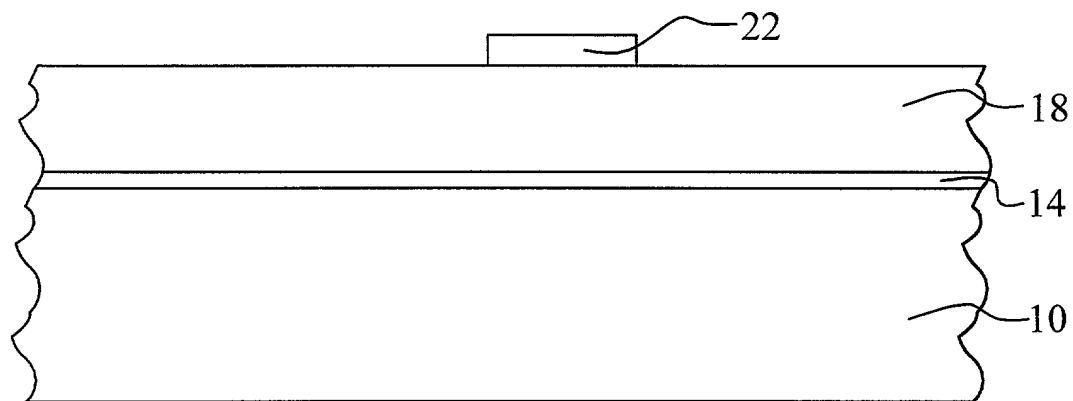


FIG. 4 Prior Art

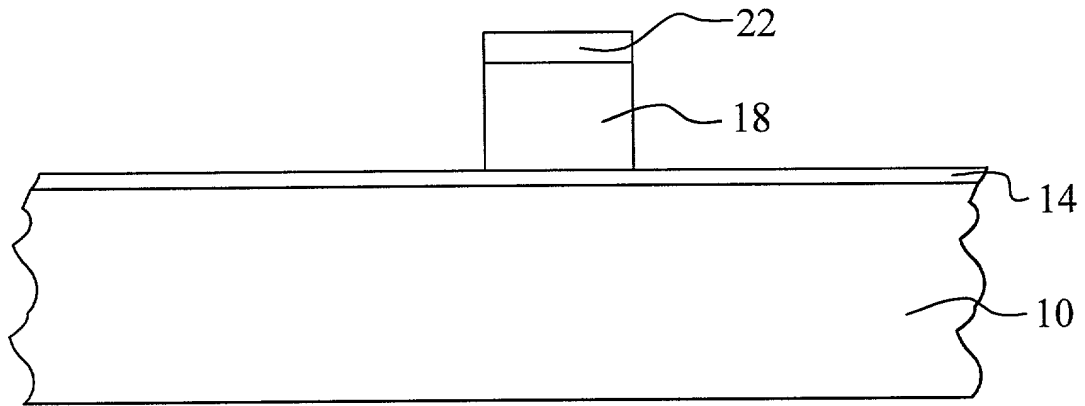


FIG. 5 Prior Art

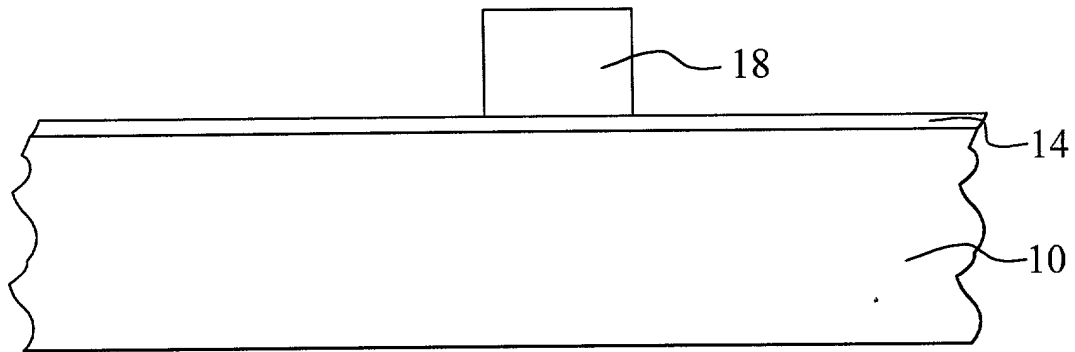


FIG. 6 Prior Art

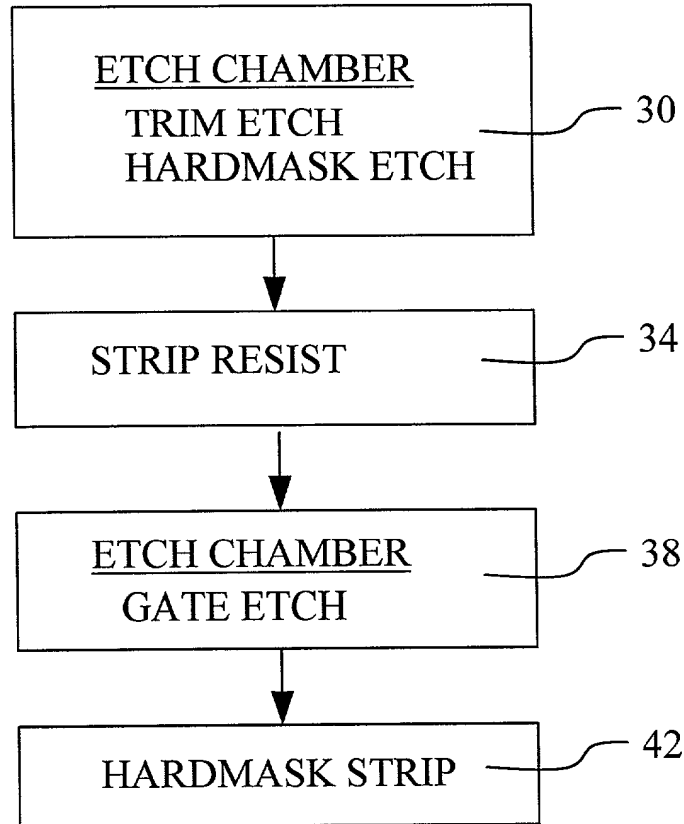


FIG. 7 Prior Art

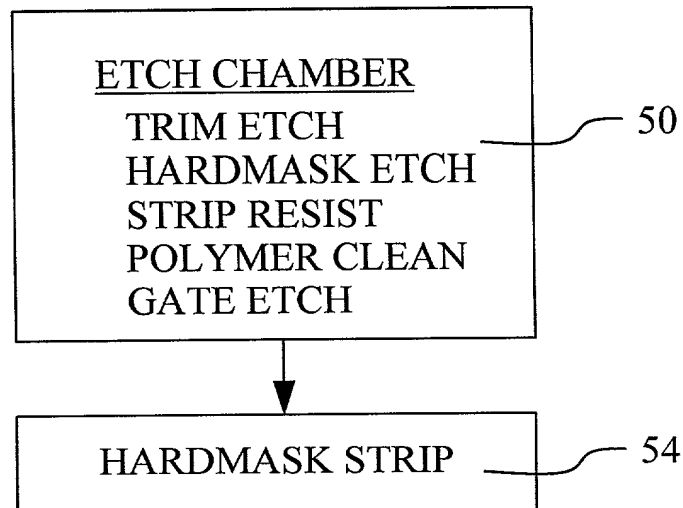


FIG. 8

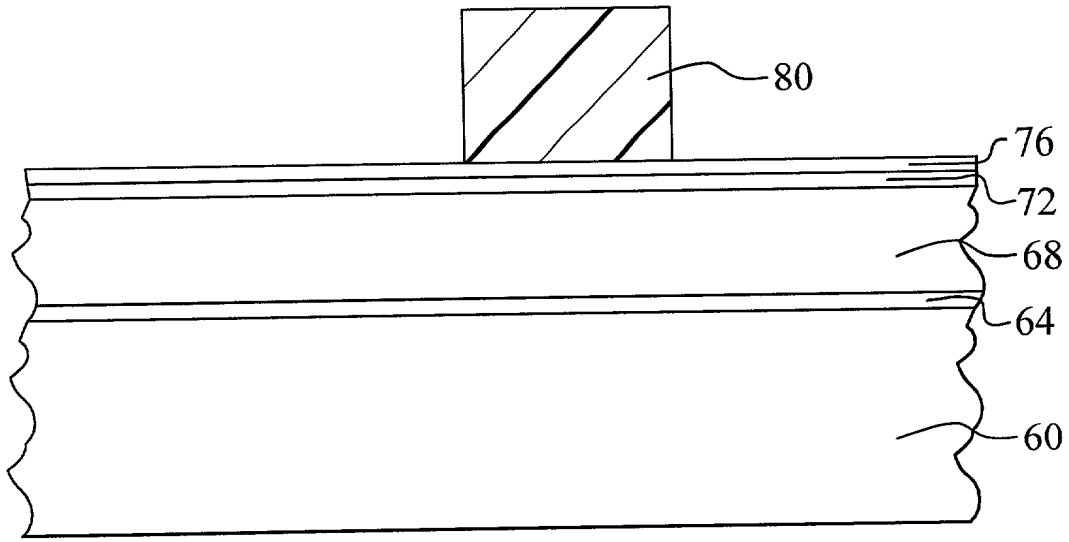


FIG. 9

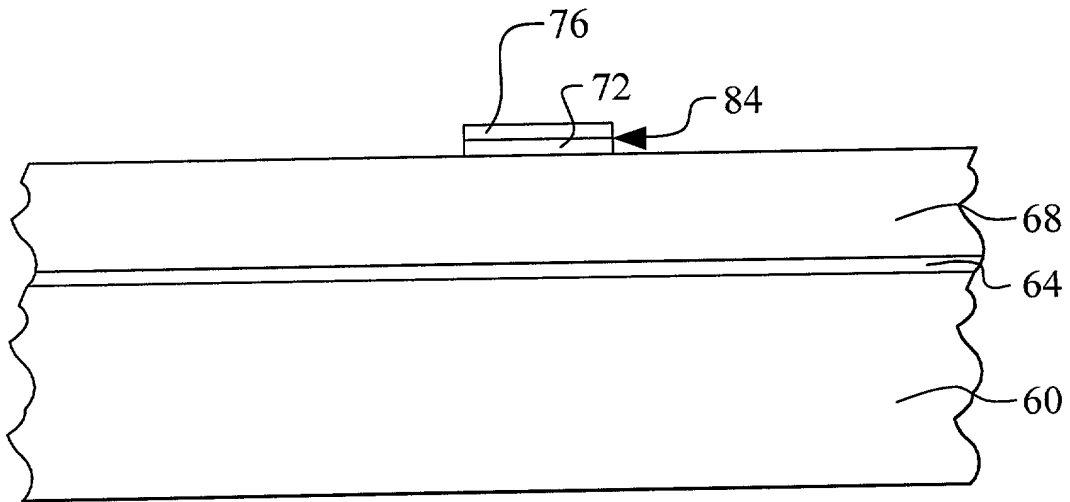


FIG. 10

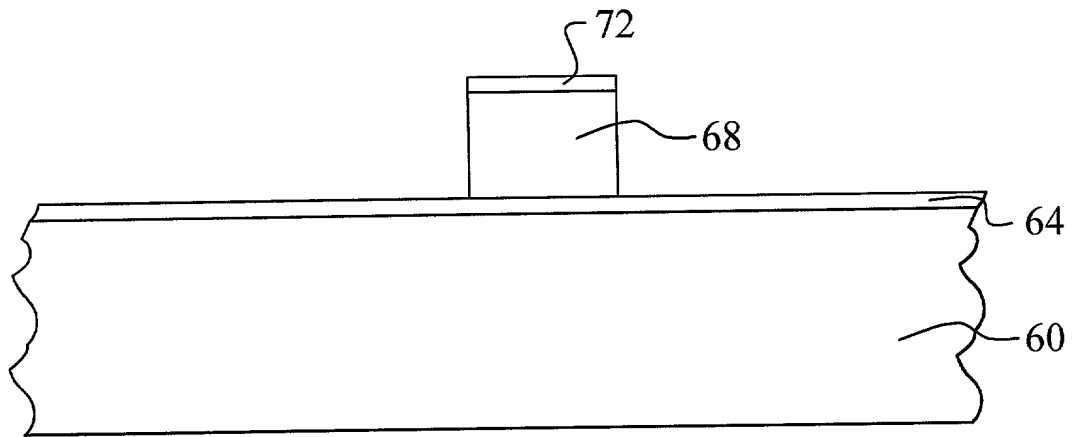


FIG. 11

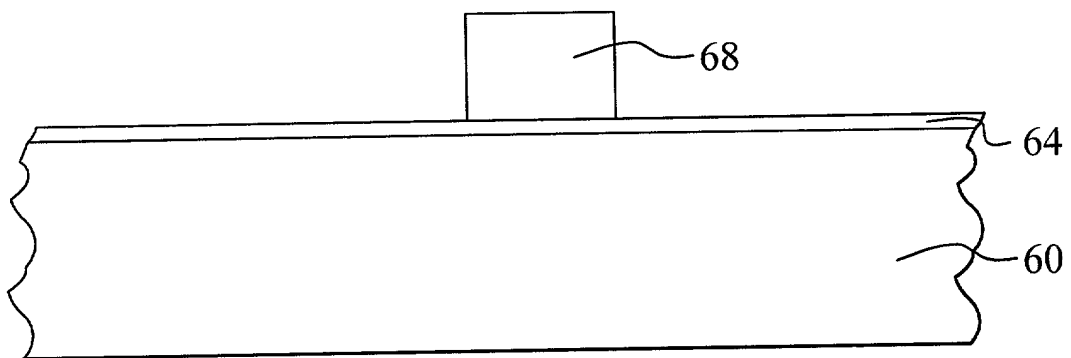


FIG. 12

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

DOCKET NO. TSMC2000-143

As a below named Inventor, I hereby declare that:

SEP 25 2000

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
An In-Situ Strip Process For Polysilicon Etching In Deep Sub-Micron Technology

the specification of which (check one)

X is attached hereto.

was filed on _____

Application Serial No. _____

and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above Identified specification including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

Priority Claimed:

(Number)	(Country)	(Day/Month/Year Filed)
(Number)	(Country)	(Day/Month/Year Filed)

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name & registration no.)

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